

Young-Ho Gong

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Work EXPERIENCE

Samsung Electronics Co. Ltd, Memory Business, Hwaseong, South Korea

September 2018 **Senior Engineer (CL3)**

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• Controller Development Team

Korea University, Seoul, Korea

March 2012 **Research Assistant**

~ August 2018
• Research on Monolithic 3D-based Cache Architecture [ISLPED'17]
• Research on Mobile AP Thermal Modeling and Validation [IEEE D&T'18]
• Research on Low-power DRAM Refresh [MICPRO'17], [IEEE TC'16], [MICPRO'16]
• Research on Low-power Hybrid Cache Architecture [ISQED'13]

Georgia Institute of Technology, GA, USA

February 2013 **Visiting Student (funded by BK21 project)**

• Research on Thermal Behavior of 3D-MAPS

HONORS & AWARDS

Research Grant 2017 Research Excellence Award,
Dept. of Computer Science and Engineering, Korea University

RESEARCH INTEREST

Cache Architecture Monolithic 3D-based Cache Architecture [ISLPED'17]

Low-power Hybrid Cache Architecture [ISQED'13]

Low-power DRAM Low-power DRAM Refresh Technique [MICPRO'17], [IEEE TC'16]
Thermal-aware Refresh Technique for 3D eDRAM stacked Caches [MICPRO'16]

Thermal-aware Design Mobile AP Thermal Modeling and Validation [IEEE D&T'18]

PUBLICATION

International Journal Papers

1. **Young-Ho Gong**, J. Kong, and Sung Woo Chung,
"Quantifying the Impact of Monolithic 3D (M3D) Integration on L1 Caches," IEEE Transactions on Emerging Topics in Computing, *under review* (**IF:3.626**)
2. **Young-Ho Gong**, J. J. Yoo, and Sung Woo Chung,
"Thermal Modeling and Validation of A Real-World Mobile AP," IEEE Design & Test, *vol.35, no.1, pp.55-62, February 2018* (**IF:1.538**)
3. J. Kong and **Young-Ho Gong (First Student Author)**,
"An Efficient Trade-Off between Yield and Energy for eDRAM Caches under Process Variations," Microprocessors and Microsystems, *vol.55, November 2017*. (**IF:1.049**)
4. J. Kong, **Young-Ho Gong (First Student Author)**, and Sung Woo Chung,
"Towards Refresh-optimized EDRAM-based Caches with a Selective Fine-grain Round-robin Refresh Scheme," Microprocessors and Microsystems, *vol. 49, pp. 95-104, March 2017*. (**IF:1.049**)

5. **Young-Ho Gong** and Sung Woo Chung,
“Exploiting Refresh Effect of DRAM Read Operations: A Practical Approach to Low-power Refresh,” IEEE Transactions on Computers, *vol. 65, no. 5, pp. 1507-1517, May 2016. (IF:3.052)*
6. **Young-Ho Gong**, J. M. Kim, S. K. Lim, and Sung Woo Chung,
“Exploration of Temperature-aware Refresh Schemes for 3D Stacked eDRAM Caches,” Microprocessors and Microsystems, *vol. 42, pp. 100-112, May 2016. (IF:1.049)*

International Conference Papers

1. **Young-Ho Gong**, J. J. Yoo, and Sung Woo Chung,
“Thermal Modeling and Validation of A Real-World Mobile AP,” IEEE Int’l Symposium on Circuits and Systems (ISCAS), May 2018. (*presented in CAS-T session*)
2. J. Kong, **Young-Ho Gong (First Student Author)**, and Sung Woo Chung,
“Architecting Large-scale SRAM Arrays with Monolithic 3D Integration,” IEEE Int’l Symposium on Low Power Electronics and Design (ISLPED), July 2017. (*regular paper acceptance rate: 25.6%*)
3. **Young-Ho Gong**, H. B. Jang, and Sung Woo Chung,
“Performance and Cache Access Time of SRAM-eDRAM Hybrid Caches Considering Wire Delay,” Int’l Symp. on Quality Electronic Design (ISQED), March 2013. (*regular paper acceptance rate: 36.3%*)

PATENT

International Patents

1. Sung Woo Chung, **Young-Ho Gong**, Jae Hoon Chung, and Hoon Hee Cho
“Hybrid memory system and control method thereof,”
United States Application Number: 15/702499, September 2017

Domestic Patents

1. Sung Woo Chung, **Young-Ho Gong**, and Sang Jun Nam
“Monolithic 3D-based Neuromorphic Chip”
Korea Application Number: 10-2018-0015670, February 2018
2. Sung Woo Chung and **Young-Ho Gong**,
“Monolithic 3D-based Cache Memory Architecture,”
Korea Registration Number: 10-1780586, September 2017.
3. Sung Woo Chung and **Young-Ho Gong**,
“Monolithic 3D-based Page Table Architecture for Main Memory Systems,”
Korea Registration Number: 10-1771350, August 2017.
4. Sung Woo Chung and **Young-Ho Gong**
“Monolithic 3D-based Cache Memory Architecture and Control Method Thereof,”
Korea Application Number: 10-2017-0096900, July 2017
5. Sung Woo Chung, **Young-Ho Gong**, and Joonho Kong
“Monolithic 3D-based Cache Memory Architecture,”
Korea Application Number: 10-2017-0024233, February 2017
6. Sung Woo Chung and **Young-Ho Gong**,
“Monolithic 3D-based Cache Memory Architecture,”
Korea Application Number: 10-2017-0024232, February 2017
7. Sung Woo Chung and **Young-Ho Gong**,
“Memory Refresh Technique,”
Korea Application Number: 10-2014-0115368, September 2014.

PROFESSIONAL EXPERIENCE

Reviewer IEEE ACM/EDAC/IEEE Design Automation Conference (DAC) 2017, 2018
IEEE Int'l Symposium on Low Power Electronics and Design (ISLPED) 2016,2018
IEEE Int'l Conference on Computer Design (ICCD) 2012, 2013.
IEEE Transactions on Computers (TC)

Teaching EXPERIENCE

Teaching Assistant Computer Architecture (2012 Fall, 2013 Fall), Logic Design (2013 Spring)

SKILL

Simulation & Modeling **Architectural Performance/Power Simulation**
• Gem5, MARSSx86, Pintool, GPGPU-sim, Macsim, Wattch, etc.
Memory Latency/Power/Area Simulation/Modeling
• CACTI, CACTI-3DD, Destiny, NVSim, DRAMSim2, etc.
Thermal Simulation/Modeling
• HotSpot (*not only simulation, but also modeling (including 3D thermal modeling)*)

Language C/C++, Verilog HDL, Java, Python, etc.

EDUCATION

Korea University, Seoul, Korea

March 2012 ~ August 2018 **Ph. D. in Computer Science (The Integrated Master & Ph. D. Course)**

- Advisor: Prof. Sung Woo Chung
- *Thesis: Thermal-/Energy-aware Architectural Design Techniques*

March 2008 ~ February 2012 **B. S. in Computer & Communication Engineering**

- Classes: Computer architecture, Operating system, Computer system, Logic design and experiment, Multimedia programming, Algorithm, etc.

REFERENCE

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Professor

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Prof. Sung Kyu Lim

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