Jae Yoon Lee

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Research Interests

Dynamic Thermal Management, Error Correction Codes, Thermal Modeling

Education

Korea University Mar. 2023 – Feb. 2028 (Expected)
Ph.D. in Computer Science and Engineering *Seoul, Korea*

- Advised by Professor Sung Woo Chung
- GPA: 4.1/4.5
- Coursework: Computer Architecture and Systems, Microprocessor Architecture, etc.

Korea University Mar. 2016 – Aug. 2022
B.S. in Computer Science and Engineering *Seoul, Korea*

- Two-year break for military service (Feb. 2018 - Oct. 2019)
- GPA: 3.83/4.5 (Major GPA: 3.98/4.5)
- Coursework: Computer Architecture and Systems, Operating Systems, Computer Network, etc.

Publications

Jae Yoon Lee, Chae Young Sim, Seung Hun Choi, and Sung Woo Chung, **"Thermal Challenges and Opportunities for Off-the-shelf 3D-stacked CPUs,"** *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2025.

Jae Yoon Lee, Young Seo Lee, Young-Ho Gong, Seon Wook Kim, and Sung Woo Chung, **"SHIFT ECC: A Value Converting HBM ECC Approach for Refresh Energy Efficient Integer Quantized DNN Inference,"** *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2025.

Jae Yoon Lee and Sung Woo Chung, **"Thermal Simulation of ML Applications on a Commercial DRAM-based PIM,"** *International Technical Conference on Circuits/Systems, Computers, and Communications (ITC-CSCC)*, 2024.

(Domestic) Chae Young Sim, **Jae Yoon Lee**, and Sung Woo Chung, **"Performance Comparison of Heterogeneous Cores in Mobile APs under Thermal Constraints,"** *Korea Computer Congress (KCC)*, 2025.

(Domestic) **Jae Yoon Lee**, Jeongsu Kim, Kyungwoon Lee, and Chuck Yoo, **"Network Performance Evaluation on Secure Container Runtimes,"** *Korea Computer Congress (KCC)*, 2021.

Research Experience

Research Assistant Mar. 2023 – Current
SoC & Microprocessor Research Lab. (Advisor: Professor Sung Woo Chung) *Seoul, Korea*

- Designed an error correction codes (ECC) for energy-efficient and accurate integer quantized DNN inference on HBM, leveraging the retention error characteristics. (supported by *Samsung Electronics System LSI*)
- Conducted power and thermal simulations of an off-the-shelf processing-in-memory (PIM) device (SK hynix GDDR6-AiM) for various DNN inference workloads using gem5-Aladdin, DRAMsim3, and HotSpot 6.0. (supported by *SK hynix* and *IITP*)
- Designed a high-performance dynamic thermal management (DTM) technique for CPU-NPU systems, exploiting the instruction complexity of software-defined robotics (SDR) workloads. (supported by *IITP*)
- Designed OS-level thermal-aware task scheduling techniques for high-performance CPUs, leveraging the floorplan and adaptive voltage scaling (AVS). (supported by *IITP*)

Undergraduate Researcher Jul. 2022 – Feb. 2023
SoC & Microprocessor Research Lab. (Advisor: Professor Sung Woo Chung) *Seoul, Korea*

- Analyzed the retention error characteristics under various ambient temperatures by modifying the memory controller RTL for SDR SDRAM (Nios II, Altera Quartus II) and DDR4 SDRAM (Arm Cortex-A72, Xilinx Vivado). (supported by *IITP*)

Undergraduate Researcher Jan. 2021 – Dec. 2021
Operating Systems Lab. (Advisor: Professor Chuck Yoo) *Seoul, Korea*

- Analyzed the network performance overhead of Docker (bridge), Kata Containers (vhost), and Firecracker (VirtIO) using Netperf and Linux perf. (supported by *IITP* and *NRF*)

Patents

(Domestic) Sung Woo Chung and **Jae Yoon Lee**, **"Error Correction Code Circuit and Memory Device,"** *Korea Application Number: 10-2025-0071388*, 2025.

Professional Experience

Reviewer 2024 – 2025

- *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*

Teaching Assistant Fall 2024
Computer Architecture (Instructor: Professor Sung Woo Chung) *COSE222*

- Undergraduate course (60+ students).
- Gave six 1.25 hour lectures on basics of Verilog HDL, logic synthesis, and functional/timing simulation using an Altera DE2 FPGA board.
- Designed several Verilog HDL coding assignments (combinational/sequential circuits, RISC-V single-cycle processor, and RISC-V multi-cycle processor).

Teaching Assistant Spring 2024
Computer Architecture (Instructor: Professor Sung Woo Chung) *COSE222*

- Undergraduate course (15+ students).
- Gave six 1.25 hour lectures on basics of Verilog HDL, logic synthesis, and functional/timing simulation using an Altera DE2 FPGA board.
- Designed several Verilog HDL coding assignments (combinational/sequential circuits, RISC-V single-cycle processor, and RISC-V multi-cycle processor).

Teaching Assistant Fall 2023
Logic Design (Instructor: Professor Sung Woo Chung) *COSE221*

- Undergraduate course (80+ students).
- Gave six 1.25 hour lectures on basics of Verilog HDL, logic synthesis, and functional/timing simulation using an Altera DE2 FPGA board.
- Designed several Verilog HDL coding assignments (combinational/sequential circuits, general purpose input/output (GPIO), and finite state machines (FSMs)).

Technical Skills

Programming Language

- Advanced: C, Python, Shell, Verilog HDL, Assembly (ARMv7)
- Moderate: C++, Assembly (ARMv8, RISC-V)
- Novice: Java

Framework and Tool

- Advanced: PyTorch, Quartus
- Moderate: Vivado, Vitis
- Novice: TensorFlow

References

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