

Young Seo Lee

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RESEARCH INTEREST

- 3D Stacked Architecture [DAC'19][INTEGRATION'21][IEEE ESL'21][IEEE Access'21]
- Processing-in-Memory Architecture in High Bandwidth Memories [ICCD'19][IEEE ESL'21]
- Reliable Memory Systems [DATE'22]
- OS-level Energy Management Techniques [IEEE TC'20]

RESEARCH EXPERIENCE

Korea University, Korea

3/2018 ~ 8/2022 **Research Assistant**

- Leading a Project for In-Memory Accelerators for Emerging Memory Systems.
 - “In-Memory Accelerators Using Next Generation Memories Based on Their Characteristics,” supported by NRF (Program: Research Subsidies for Ph.D. Candidates).
- Participated in 2 Projects for Architecting In-Memory Accelerators.
 - “Thermal Aware In-Memory Accelerators Based on 3D Stacked Memories,” supported by NRF.
 - “PIM Core Technology and System Development for Data-intensive Applications,” supported by Samsung Electronics’ Memory Division.
- Participated in a Project for Reliable Memory Systems.
 - “DRAM Based Memory Hierarchy Design and Application,” supported by Samsung Electronics’ Memory Division.
- Participated in 6 Projects for Power/Thermal Analysis on 3D Stacked Architectures.
 - “System-level Thermal Management Technique for 2.5D and 3D Stacked Structures considering the Surrounding Environment,” supported by Samsung Electronics’ System LSI.
 - “Development of Thermal Management Technique for Supercomputer CPU,” supported by NRF.
 - “Development of Low Temperature Process Based M3D Integration Device and Circuit Platform with Si/SiGe Layer,” supported by NRF.
 - “Designed Architecture Considering Application Characteristics and Process Technology,” supported by Samsung Electronics’ System LSI.
 - “System-Level Design and Analysis Platform for Neuromorphic Interconnects with Monolithic 3D,” supported by NRF.
 - “Monolithic 3D Integration Architecture and Process Development for Low Power IoT Device Platform,” supported by NRF.
- Participated in a Project for Power/Thermal Management for Datacenters.
 - “Development of Energy-/Thermal- Optimal System SW in a Single Node,” supported by NRF.

3/2017 ~ 2/2018 **Undergraduate Research Intern**

- Participated in a Project for Power/Thermal Management for Datacenters
- Designed an ARM-compatible Microprocessor with Verilog HDL

PUBLICATION

International Journal Papers

1. **Young Seo Lee**, Y.-H. Gong, and Sung Woo Chung, “Scale-CIM: Precision-scalable computing-in-memory for energy-efficient quantized neural networks,” in *Journal of Systems Architecture (IF: 5.836)*, under review.
2. **Young Seo Lee**, E.-Y. Chung, Y.-H. Gong, and Sung Woo Chung, “Quant-PIM: An energy-efficient processing-in-memory accelerator for layer-wise quantized neural networks,” *IEEE Embedded Systems Letters*, vol. 13, no. 4, pp. 162-165, December 2021. (*IF: 1.524*)
3. J. H. Lee, **Young Seo Lee**, J. H. Choi, H. Amrouch, J. Kong, Y.-H. Gong, and Sung Woo Chung, “Characterizing the thermal feasibility of monolithic 3D microprocessors,” *IEEE Access*, vol. 9, pp. 120715-120729, August 2021. (*IF: 3.476*)
4. C. T. Do, J. H. Choi, **Young Seo Lee**, C. H. Kim, and Sung Woo Chung, “Enhancing matrix multiplication with a monolithic 3D based scratchpad memory,” *IEEE Embedded Systems Letters*, vol. 13, no. 2, pp. 57-60, June 2021. (*IF: 1.524*)

5. **Young Seo Lee**, K. M. Kim, J. H. Lee, Y.-H. Gong, S. W. Kim, and Sung Woo Chung, “Monolithic 3D stacked multiply-accumulate units,” *Integration the VLSI Journal*, vol. 76, no. 1, pp. 183-189, January 2021. (**IF: 1.345**)
6. Y. G. Kim, **Young Seo Lee**, and Sung Woo Chung, “Signal strength-aware adaptive offloading with local image preprocessing for energy efficient mobile devices,” *IEEE Transactions on Computers*, vol. 69, no. 1, pp. 99-111, January 2020. (**IF: 3.183**)

International Conference Papers

1. **Young Seo Lee**, G. Koo, Y.-H. Gong, and Sung Woo Chung, “Stealth ECC: A data-width aware adaptive ECC scheme for DRAM error resilience,” in *Design, Automation and Test in Europe (DATE)*, March 2022. (**Regular paper acceptance rate: 25.0%, DATE is recognized as a journal of SCI IF 2 by Korean Institute of Information Scientists and Engineers**)
2. **Young Seo Lee**, K. M. Kim, J. H. Lee, J. H. Choi, and Sung Woo Chung, “A high-performance processing-in-memory accelerator for inline data deduplication,” in *IEEE International Conference on Computer Design (ICCD)*, November 2019. (**Regular paper acceptance rate: 23.8%, ICCD is recognized as a journal of SCI IF 1 by Korean Institute of Information Scientists and Engineers**)
3. **Young Seo Lee**, K. M. Kim, S. J. Nam, Y. H. Gong, S. W. Kim, and Sung Woo Chung, “A high speed multiply-accumulate unit: Case studies on 3D stacked FPGA and ASIC,” in *Design Automation Conference (DAC)*, June 2019. (**poster (DAC is recognized as a journal of SCI IF 3 by Korean Institute of Information Scientists and Engineers)**)

PATENTS

Domestic Patents

1. **Young Seo Lee**, T. C. Do, and Sung Woo Chung, “A GPU cache bypassing method and apparatus with the adoption of monolithic 3D based network-on-chip” Korea Registration Number: 10-2340444, December 14, 2021.
2. **Young Seo Lee**, T. C. Do, and Sung Woo Chung, “Monolithic 3D integration based on L1 cache memory for GPUs,” Korea Registration Number: 10-2172556, October 27, 2020.
3. **Young Seo Lee**, Y. G. Kim, and Sung Woo Chung, “Method for predicting CPU temperature based on machine learning,” Korea Registration Number: 10-2123178, June 9, 2020.
4. **Young Seo Lee** and Sung Woo Chung, “Memory system including data-width aware encoder and data-width aware decoder and operating method thereof,” Korea Application Number: 10-2022-0021042, February 17, 2022.
5. **Young Seo Lee**, Y.-H. Gong, and Sung Woo Chung, “Precision-scalable computing-in-memory for quantized neural networks,” Korea Application Number: 10-2022-0018230, February 10, 2022.
6. **Young Seo Lee**, Y.-H. Gong, and Sung Woo Chung, “In-memory accelerator for layer-wise quantized neural networks and operation method thereof,” Korea Application Number: 10-2021-0020195, February 16, 2021.
7. **Young Seo Lee**, T. C. Do, J. H. Choi, and Sung Woo Chung, “A monolithic 3D based scratchpad memory,” Korea Application Number: 10-2021-0017652, February 8, 2021.

HONORS & AWARDS

Best Paper Awards (4 th place)	“Stealth ECC: A data-width aware adaptive ECC scheme for DRAM error resilience,” 2021 Samsung Humantech Paper Award, Computer Science & Engineering
Best Awards (2 nd place)	“Signal strength-aware adaptive offloading for energy-efficient edge computing,” 2017 Graduation Project Competition, Dept. of Computer Science and Engineering, Korea University

Best Awards (4 th place)	"Scrapper: An Application that allows you to scrap and organize articles you want" 2017 iOS Application Development Hackathon, Korea University
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PROFESSIONAL EXPERIENCE

Reviewer	IEEE International Symposium on High-Performance Computer Architecture (HPCA) 2022 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED) 2018-2022 The International Symposium on Memory Systems (MEMSYS) 2019
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EXPERTISE

Programming Language	C/C++, Verilog HDL, Java, Assembly (ARM, MIPS, x86), Python, Android, Swift
Tools for FPGA/ASIC	Altera Quartus, Design Compiler, IC Compiler
Etc.	Design & Implementation of FIM System with HBM Design & Implementation of Linux Task Scheduler Analysis on Power/thermal Management Techniques Completion of the "Design Compiler Training Course" conducted by ETRI (Electronics and Telecommunications Research Institute)

EDUCATION

Korea University, Seoul, Korea

3/2018 ~ 8/2022 **Ph. D. in Computer Science (The integrated Master & Ph. D. Course)**

- Thesis: Architecture-Level Techniques for Intelligent/Reliable Memory Systems
- Advisor: Prof. Sung Woo Chung

3/2013 ~ 2/2018 **B. S. in Computer Science**

- Classes: Computer Architecture, Operating Systems, Computer Systems, System Software Design and Experiment, Logic Design and Experiment, Algorithm, Compiler, etc.

REFERENCE

Prof. Sung Woo Chung

Professor

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